



Various Authors

NMRA Standard	
DCC Service Mode Programming.	
Sep 1, 2026	S-9.2.3 Draft

1 General

1.1 Introduction and Intended Use (Informative)

The NMRA Standards and Recommended Practices for Digital Command Control (DCC) define two modes of Digital Decoder operation: Operations Mode and Service Mode. This STANDARD describes Service Mode. The purpose of Service Mode is to allow customization and testing of Digital Decoders.

1.2 References

This standard should be interpreted in the context of the following NMRA Standards, Technical Notes, and Technical Information.

1.2.1 Normative

- NMRA S-9.2 DCC Communications Standard
- NMRA S-9.2.1 DCC Extended Packet Formats
- NMRA S-9.2.2 DCC Configuration Variables
- NMRA S-9.3.2 DCC Basic Decoder Transmission

1.2.2 Informative

- RailCommunity RCN-216 DCC Programming Environment
- RailCommunity RCN-214 DCC Protocol Configuration Commands
- RailCommunity RCN-211 DCC Packet Structure and Address Ranges

1.3 Terminology

Term	Definition
Digital Decoder	DCC receiver for controlling the vehicle.
Service Mode	A special DCC operating mode for customization and setup of a Digital decoder away from the layout operational environment.
Programmer	A device which may or may not be part of a DCC Command station which is used to communicate in Service Mode with a Digital decoder.

2 Service Mode Environment

Service Mode is designed for testing and customization of Digital Decoders. It is recommended that:

- 25 1) Service Mode operations should occur on an isolated section of track.
- 2) External locomotive loads (i.e. smoke generator, constant lighting, and sound generators) should be switched off during programming operations. Decoders should be able to switch off all external loads connected to the decoder upon entering service mode.
- 30 3) Service Mode operations should be performed in an environment with limited energy to prevent damage to decoders during programming. For the purposes of this STANDARD, limited energy is defined as 100 mA, sustained for more than 100ms.

A Programmer is the device used to create these conditions and may be incorporated within or separate from the system Digital Command Station.

3 Digital Decoder Entry to and Exit from Service Mode

- 35 A Digital Decoder will only act on service mode instruction packets while in service mode.

A Digital Decoder will enter service mode upon receipt of a reset packet followed by a valid service mode instruction packet. Valid service mode packets are described in Section 5.

A Digital Decoder will exit service mode but not enter operations mode when any of the following conditions are true:

- 40 1) The Digital Decoder successfully receives a non-service-mode instruction packet.
- 2) 20 milliseconds have occurred since the last valid reset or service mode instruction packet was received.

Once a Digital Decoder has exited service mode, it will only re-enter operations mode upon receipt of a valid operations mode packet that is not identical to a service mode packet. This is to ensure that the decoder does not start executing service mode instruction packets as operations mode packets. Service Mode instruction packet formats have a value in the range 112 to 127 in the byte defined as short address in operations mode packets.

3.1 Decoder Acknowledgment Mechanism

Service Mode operations provide for an acknowledgment mechanism from the decoder to the command station/programmer. Acknowledgment refers to the ability of the Digital Decoder to respond to a Service Mode instruction issued by a Programmer. Service Mode instructions can be executed regardless of whether or not the acknowledgment mechanism is detected by the command station/programmer.

Two Acknowledgment mechanisms are available:

- 55 -Basic Acknowledgment
-Advanced Acknowledgment

Digital Decoders may provide either form of acknowledgment.

3.1.1 Basic Acknowledgment

Basic acknowledgment is defined by the Digital Decoder providing an increased load (positive-delta) on the programming track of at least 60 mA for 6 ms +/-1 ms. It is permissible to provide this increased load by applying power to the motor or other similar device controlled by the Digital Decoder.

3.1.2 Advanced Acknowledgment

See NMRA S-9.3.2.

Commented [MM1]: Is Railcom acknowledgement allowed in Service Mode; I thought it wasn't. S-9.3.2 revision Sept 2026 states (line 25) that it is not currently supported. So the question is, what is Advanced Acknowledgement? Is this to be removed?

Commented [MJ2R1]: That is a Brian Kopp question.

65 **3.1.3 General Acknowledgment timing**

For either type of Acknowledgment, if a Service Mode Write is being performed, Acknowledgment pulse(s) should not occur from the decoder until internal updating of all affected non-volatile data storage is complete in the decoder. During Service Mode the Programmer should scan for any Acknowledgment current pulse(s) in the Acknowledgment time window starting at the Packet End bit of the second service mode instruction packet and extending through the required number of instruction packets and in the case of write operations through the specified decoder-recovery-time.

70 A Command Station/Programmer may not stop sending packets to the programming track (which may turn off power to the decoder) until the end of the Decoder-Recovery-Time.

4 Service Mode Instruction Packets

75 Service Mode supports four different methods for access to Configuration Variables (CVs):

- Direct Configuration,
- Address-Only,
- Physical Register,
- Paged Addressing.

80 The Service Mode instruction packet sequences are defined from a Command Station/Programmer perspective. A Digital Decoder must not execute any Verify or Write operations (as specified herein) unless it is in service mode (see section 3) and has received two identical Service Mode packets without any intervening valid packets. Digital Decoders must successfully perform the desired programming operation, including performing its acknowledgment function, if required, within the time frame defined by this packet sequence.

85 Whichever mode is used, whenever a change to CV #1 – the Short Address – is made, the decoder must also:

- reset the extended addressing bit in the Configuration Register CV #29 to have a value of '0' (zero)
- clear the consist address (CV #19) to a value of '0' (zero)

Commented [MM3]: I've moved this from the Address Mode description, because it said there that this provision actually applied to all modes. I think this helps to make that clearer,

Commented [MJ4R3]: Agreed

4.1 Definitions

Within this standard, bits are numbered from right to left with bit 0 (the right most bit) being the least significant bit (LSB) and bit 7 (the left most bit) being the most significant bit (MSB). Bits will be defined using the following abbreviations:

- 95
- | | |
|---|------------------------------------|
| 0 | bit with a value of "0" |
| 1 | bit with a value of "1" |
| A | the configuration variable address |
| C | instruction type |
| K | instruction type |
| R | register number |
| B | position of bit |

- D data value to be read or written
- E error detection bit ¹
- [] sequences between braces may be repeated, and nested one or more times as needed

100 **Long Preamble** - In Service Mode the Command Station/Programmer will increase the preamble of the packet from the minimum (per S-9.2) to at least 20 bits to allow extra time for the Digital Decoder to process the packets. This is designated as "long-preamble" in the packet descriptions within this Standard.

105 **Power-On Cycle** - Upon applying power to the track, the Command Station/Programmer must transmit at least 20 valid packets to the Digital Decoder to allow it time to stabilize internal operation before any Service Mode operations are initiated. During the initial decoder power-up sequence, a current load of greater than 250 mA sustained after 100 milliseconds (ms) of initiation of packet transmission should be interpreted as an over-current fault condition for the decoder being programmed. After the power-up sequence, a decoder with all outputs turned off (i.e. lamps, amplifiers, etc.) shall not draw more than 100 mA of current except for when processing an acknowledgment.

110 **Decoder Recovery Time** - Command Station/Programmer shall send the same service mode write packets or reset packets during the Decoder-Recovery-Time until the specified packet time has been met or the until the command station/programmer has received a valid acknowledgment.

Reset Packet - Herein, a reset packet is defined as a Broadcast Decoder Reset packet, valid for all decoders (see S-9.2).

115 **Hard-Reset-Cycle** - A hard reset (see S-9.2.1), followed by 10 idle or reset packets. This sequence is used when a Command Station/Programmer desires to return the decoder to its initial predefined state.

Page-Preset-Instruction - A packet sequence sent to guarantee the contents of the page register. The instruction sequence is (long-preamble 0 01111101 0 00000001 0 01111100 1)²

120 4.2 Service Mode Instruction Packets for Direct Mode

Direct Mode service mode instruction packets support accessing Configuration Variables by their configuration variable number (see S-9.2.2).

125 To determine if a Digital Decoder supports Direct Configuration Variable Addressing, the Universal Command Station/Programmer should perform two bit verifies, one verify for a bit value of '0', one verify for a bit value of '1' to the most significant bit within CV #8 (Manufacturer's ID). Acknowledgment of either bit-verify indicates that the decoder fully supports all modes of Direct Configuration Variable Addressing (Verify Byte, Write Byte, & Bit Manipulation). A Command Station, Programmer, or Decoder, which supports Direct Mode must implement all three instruction-types.

130 The following table shows the required packet sequence for direct mode.

¹In both the three (3) data byte and the four (4) data byte packets, the last data byte of a Service Mode packet is used for error detection purposes. See S-9.2.1 for details of the error correction byte.

² This instruction may not have the desired effect with all older accessory decoders.

Packet Sequence for Command Stations/Programmers using Direct Mode

Optional Power-On-Cycle, if needed	
3 or more Reset Packets	
Either:	Or:
5 or more Verify packets to a single CV 1-1023, followed by 1 or more Reset Packets, if an acknowledgement is detected	5 or more Writes to a single CV 1-1023
	6 or more Identical Write or Reset packets (Decoder-Recovery-Time)
Optional Power-Off	

Within a verify or write sequence, the Command Station/Programmer may cease sending packets and continue with the next step in the sequence when either a decoder acknowledgment is successfully received, or the number of packets specified to be transmitted is completed.

Instruction packets using Direct CV Addressing are 4 byte packets of the format:

Long-preamble 0 0111CCAA 0 AAAAAAAAA 0 DDDDDDDD 0 EEEEEEEE 1

The actual Configuration Variable desired is selected via the 10 bit address with the two bit address (AA) in the first data byte being the most significant bits of the CV number. The Configuration variable being addressed is the provided 10 bit address plus 1. CV #1 is defined by the address 00000000. A Command Station/Programmer must provide full read and write manipulation for all values of 8 bit data.

The defined values for Instruction types (CC) are:

CC=10 Bit Manipulation

CC=01 Verify byte

CC=11 Write byte

CC="01" VERIFY CV BYTE

The contents of the Configuration Variable as indicated by the 10 bit address are compared with the data byte (DDDDDDDD). If the values are identical the Digital Decoder shall respond with an acknowledgment as defined in Section 3.

CC="11" WRITE CV BYTE

The contents of the Configuration Variable as indicated by the 10 bit address are replaced by the data byte (DDDDDDDD). Upon completion of all write operations, the Digital Decoder may respond with an acknowledgment as defined in Section 3.

- 160
- CC="10" CV BIT MANIPULATION
- The Bit Manipulation instructions in Direct Addressing mode use a special format for the data byte DDDDDDDD:
- long-preamble 0 011110AA 0 AAAAAAAAA 0 111KDBBB 0 EEEEEEEE 1
- 165
- Where BBB represents the bit position within the CV (000 being defined as bit 0) to be operated on, and D contains the value of the bit to be verified or written. K=1 signifies a "Write Bit" operation and K=0 signifies a "Bit Verify" operation.
- 170
- Each bit manipulation instruction operates in a manner similar to the VERIFY CV BYTE and WRITE CV BYTE instructions (but operates on a single bit within the CV). Using the same criteria as the VERIFY CV BYTE or WRITE CV BYTE instructions, an acknowledgment will be generated in response to a VERIFY BIT or WRITE BIT instruction if appropriate.

4.3 Service Mode Instruction Packets for Address-Only Mode

- 175
- Address-only service mode instruction packets support access to Configuration Variable #1, the Digital Decoder’s short address.

The following table shows the packet sequence.

Packet Sequence for Command Stations/Programmers using Address-only mode	
Optional Power-On-Cycle, if needed	
3 or more Reset Packets	
5 or more Page-Preset-packets	
6 or more Page Preset or Reset packets (Decoder-Recovery-Time from write to Page Register)	
Optional Power Off Followed by Power-On-Cycle	
3 or more Reset Packets	
Either:	Or:
5 or more Verifies to CV #1	5 or more Writes to CV #1
	10 or more identical Write or Reset packets (Decoder-Recovery-Time
Optional Power Off	

- 180
- Within a verify or write sequence, the Command Station/Programmer may cease sending packets and continue with the next step in the sequence when either a decoder acknowledgment is successfully received, or the number of packets specified to be transmitted is completed.

185 Instruction packets using Address-Only Mode are 3 byte packets of the format:

long-preamble 0 0111C000 0 0DDDDDDD 0 EEEEEEEE 1

In Address-Only Mode two (2) Instruction Types (C) are defined. These are:

- 190 C=0 Verify Address
C=1 Write Address

C="0" VERIFY ADDRESS CONTENTS

195 This Instruction Type causes a VERIFY operation that shall compare the eight (8) bit data value 0DDDDDDD with the contents of CV 1, the Address. If these two values are equal, the Digital Decoder shall generate an acknowledgment as defined in section 3.

C="1" WRITE ADDRESS CONTENTS

This Instruction Type causes a WRITE operation that shall store the eight (8) bit data value 0DDDDDDD into CV #1, the Address. Upon completion of all write operations, the Digital Decoder may respond with an acknowledgment as defined in Section 3.

200 **4.4 Service Mode Instruction Packets for Physical Register Addressing**

Physical Register addressing supports access to a limited number of Configuration Variables by using the internal “Registers” of a decoder. The following table shows the packet sequence.

Packet Sequence for Command Stations/Programmers using Physical Register Addressing

Optional Power-On-Cycle, if needed	
3 or more Reset Packets	
5 or more Page-Preset-packets	
6 or more reset packets (Decoder Recovery Time from write to Page Register)	
Optional Power-Off Followed by Power-On-Cycle ³	
3 or more Reset Packets	
Either:	Or:
7 or more Verifies to a specific Register	5 or more Writes to a specific Register
	6 or more identical Writes or Reset packets (Decoder Recovery Time from write to Register)
	Note: The Decoder Recovery Time is 10 packets long after a write to Register 1 (see

³ Some older decoders require a power off/on cycle at this point in order to be programmed. Power cycling at this point is not allowed if you are in the middle of a paged operation (see Service Mode Instruction Packets for Paged CV Addressing for more information.)

also Address-Only mode).

Optional Power-Off

Within a verify or write sequence, the Command Station/Programming may cease sending packets and continue with the next step in the sequence when either a decoder acknowledgment is successfully received, or the number of packets specified to be transmitted is completed.

Instructions packets using Physical Register Addressing are 3 byte packets of the format:

long-preamble 0 0111CRRR 0 DDDDDDDD 0 EEEEEEEE 1

The value encoded in bits (RRR) defines one of 8 possible Physical Registers that may be read or written by a programmer. The following table maps the Physical Registers to Configuration Variables.

Register	RRR Value	CVs for Accessory Decoders	CVs for Mobile Digital Decoders
1	000	Lower Address (CV #513)	Address (CV #1)
2	001	Undefined, see Mfg. Documentation	Start Voltage (CV #2)
3	010	Undefined, see Mfg. Documentation	Acceleration (CV #3)
4	011	Undefined, see Mfg. Documentation	Deceleration (CV #4)
5	100	Undefined, see Mfg. Documentation	Basic Configuration Register (CV #29) ⁴
6	101	Undefined, see Mfg. Documentation	(Reserved for Page Register)
7	110	Version Number (CV #7)	Version Number (CV #7)
8	111	Manufacturer ID (CV #520)	Manufacturer ID Number (CV #8)

Commented [MM5]: See the footnote below. What the heck does that footnote actually mean – as in what is an “older system” and what needs to be compatible with what in “existing decoders” – indeed, what, in this context, is an “existing decoder”?

Commented [MJ6R5]: This is needing some work. It is very confusing. Are the “older” systems still in use? Rather than existing decoders, one might say This is to preserve backward compatibility with older decoders or the installed park of decoders..

It is recommended that a Command Station/Programmer provide full read and write access to the 8 Physical registers (000) to (111) for all values of 8 bit data. This allows a user to directly manipulate Physical registers 1 (000) to 8 (111) and CV data in any manner. The Command

⁴ For compatibility with older systems, Register 5 may be used for other programming purposes when the Page Register is not equal to 1. If Register 5 is used in a different manner, it should be reset after the page register is reset to one. This is to preserve compatibility with existing decoders.

Station/Programmer documentation should indicate the numbering or name scheme in use, and how these correspond to the 8 Physical Registers.

In Physical Register Addressing Mode two (2) Instruction Types (C) are defined. These are:

- 225
- C=0 Verify register/CV contents
C=1 Write register/CV contents
C="0" VERIFY REGISTER CONTENTS
This Instruction Type causes a VERIFY operation that shall compare the eight (8) bit data value
DDDDDDDD with the contents of the specified three (3) bit register address RRR. If these two
230 values are equal, the Digital Decoder shall generate an acknowledgment as defined in section 3.
C="1" WRITE REGISTER CONTENTS
This Instruction Type causes a WRITE operation that shall store the eight (8) bit data value
DDDDDDDD into one of the eight registers as specified by the three (3) bit register address
RRR. Upon completion of all write operations, the Digital Decoder may respond with an
235 acknowledgment as defined in Section 3.

4.5 Service Mode Instruction Packets for Paged CV Addressing:

Implementations that require access to a larger number of Configuration Variables than possible using just the 8 Physical Registers, can use an extended 3-byte programming format called Paged CV addressing. If a decoder does not implement Paged CV addressing, it must not respond to Paged CV programming commands when the page register has a value greater than 1.

- 240
- Paged CV Addressing implements access to all 1024 Configuration Variables through advanced usage of the 8 Physical "registers" or storage locations. The first four registers are used as Data Registers on a particular page. The sixth register holds the current page number. The following
245 diagram shows the order of packet sequences for paged mode:

Packet Sequence for Command Stations/Programmers using Paged Mode Addressing

Optional Power-On-Cycle, if needed	
3 or more Reset Packets	
5 or more Writes to the Page Register	
6 or more reset packets (Decoder recovery Time from write to Page Register)	
3 or more Reset Packets	
Either: 5 or more Verifies to a single Data Register 1-4	Or: 5 or more Writes to a single Data Register 1-4
	6 or more identical Write or Reset packets (Decoder Recovery Time from write to Data Register)
Optional Power Off	

250 Within a verify or write sequence, the Command Station/Programming may cease sending packets and continue with the next step in the sequence when either a decoder acknowledgment is successfully received, or the number of packets specified to be transmitted is completed.

Instructions packets using Paged Mode programming are 3 byte packets of the format:

255 long-preamble 0 0111CRRR 0 DDDDDDDD 0 EEEEEEEE 1

It is recommended that a Command Station/Programmer provide full read and write manipulation for all values of 8 bit data.

260 The five (5) additional Physical registers, defined by (RRR), in use for Paged CV Addressing are:

Register	RRR Value	
1	000	Data Register 0
2	001	Data Register 1
3	010	Data Register 2
4	011	Data Register 3
5	100	Basic Configuration Register ⁵
6	101	Paging Register

265 Registers 1 through 4 (000-011) are DATA REGISTERS. They point to a set of 4 Configuration Variables as determined by the contents of the PAGING REGISTER. Register 0 points to the first CV in the set while Register 3 points to the last CV in the set.

270 Register 5 (100) is the BASIC CONFIGURATION REGISTER. This register defines the basic configuration of the Digital Decoder. See the definition of Configuration Variable 29 (S-9.2.2) for further information on the contents of this register in a Multi-function Digital Decoder and see Configuration Variable 541 (S-9.2.2) for further information on the contents of this register in an Accessory Decoder.

Register 6 (101) is the PAGING REGISTER. This register is used as an offset for the DATA REGISTERS to allow access to the larger set of 1024 configuration variables. The default value for this register is 1

⁵ Refer to the section on Physical Register addressing for other compatibility issues with the use of this register.

275 To Calculate the CV number referred to by a Data register and Page Register value:
(1) Subtract 1 from the value in the Page Register. Then multiply this value by 4.
(2) Add the number of the Data Register (000-011 or 0-3 decimal) to step (1)
(3) Add 1 to result of step (2) and this is the number of the CV being accessed.
280 The inverse of this sequence can be used to calculate the Page number and Data register for a particular CV number.
For Example: To find the Page Register and Data Register for CV 65 - Kick Start;
CV #65 - 1 = 64
64 divided by 4 = 16, 0 remainder.
16 + 1 = 17
285 Page Register 17; Data Register 0
Registers 5, 7 and 8 are unaffected by the contents of the Page Register value (see Service Mode Instruction Packets for Physical Register Addressing for more information)

In Paged CV Addressing Mode two (2) Instruction Types (C) are defined. These are:

290 C=0 Verify register/CV contents
C=1 Write register/CV contents
C="0" VERIFY REGISTER/CV CONTENTS
This Instruction Type causes a VERIFY operation that shall compare the eight (8) bit data value DDDDDDDD with the contents of the specified three (3) bit register address RRR. If these two values are equal, the Digital Decoder shall generate an acknowledgment as defined in section 3.
295 When the Register address is in the Data Register range of (000) to (011), the stored value of the CV referenced by the Data Register in combination with the Page register value will be verified.
C="1" WRITE REGISTER/CV CONTENTS
This Instruction Type causes a WRITE operation that shall store the eight (8) bit data value DDDDDDDD into one of the eight registers as specified by the three (3) bit register address RRR. Upon completion of all write operations, the Digital Decoder may respond with an acknowledgment as defined in Section 3.
300 When the Register address is in the Data Register range of (000) to (011), the CV referenced by the Data register in combination with the Page register value will be written.

305 If the decoder maintains an internal Page Register copy that is only valid when power is applied, it should NOT be initialized when a Reset packet is received. This ensures a Programmer can load the Page Register in a decoder and follow this with multiple Write and/or Verify operations while power and packets remain on.

310 To ensure compatibility with earlier Command Station/Programmers, a Command Station/Programmer should set the Page Register (101) to 'Page 1' (a data value of 1) at the end of programming. It is also recommended that decoders provide a mechanism to automatically reset

315 their page registers to have a value of 1 after programming is completed. (See Section 3: Entry to and Exit from Service Mode)

4.6 Decoder Factory Reset

320 From time to time, it may be necessary to request that the decoder reprogram all its CVs to a factory default condition. The following command sequence⁶ shall be used for this purpose. The packet sequence for this command is identical to the packet sequence specified for Service Mode Instruction Packets for Physical Register Addressing.

The instruction packets for Decoder Factory Reset are 3 byte packets of the format:

long-preamble 0 01111111 0 00001000 0 01110111 1

325 This Instruction Type causes a WRITE operation that instructs the decoder to return to a factory default condition.

330 Because the packet sequence in service mode provides insufficient time for the decoder to rewrite all its CVs, the actual reprogramming of all the decoder's CVs will normally occur during each subsequent power on cycle until such time that all CVs have been returned to a factory default condition. A value of 255 will be placed in CV8 until such time that the decoder has successfully rewritten all CVs to their factory default condition.

5 F: Methods of Programming Required

335 To conform to this STANDARD, Command Station or Programmers must implement at least one of the following groups of programming methods. The manufacturer must clearly label, using the defined terms below, which form(s) of programming are supported.

5.1 Command Station or Programmers

Address-Only Programmers	program CV #1 via Address-Only Mode
Register-Mode CV Programmers	Program a selected subset of CVs via Physical Register, subset must include CV #1 using Address Only Mode and be clearly defined and documented
Paged CV Programmers	Program a selected sub-set of CVs via Physical Register and Paged Addressing. Subset must include CV #1 using Address Only Mode and be clearly defined and documented.
Direct CV Programmers	Program a selected subset of CVs via Physical Register and Direct Addressing, subset must include CV #1 in Address-Only Mode, and be clearly defined and documented.
Universal CV Programmers	Have the ability to read and write a subset of CVs via Direct, Physical Register and Paged Addressing. Subset must include CV #1 using Address Only Mode and be clearly defined and

⁶ Several valid existing alternative means for achieving decoder factory reset are also in use. Manufacturers may continue to use these alternate means for performing factory decoder reset but are required to also support the standard specified means in new designs for achieving this result.

Commented [MM7]: See the Footnote: Do we really still require that this packet be used as a factory reset? How many DCC systems out there actually support this and can generate such packets? Is this a requirement that has passed its use-by date?

Commented [M38R7]: A good question for the WG and manufacturers specifically. It may be time to let this go.

documented.

Effective 1-Aug-2002 all Command Stations or Programmers submitted for Conformance must implement Direct Mode.

For complete backward compatibility with decoders that were produced prior to 1-Aug-2002 which do not support direct mode, support for paged mode is strongly encouraged.

5.2 Decoders

All programmable decoders must perform Address-Only mode, and either Physical Register or Paged Addressing as appropriate. Decoders that support Service Mode programming for more CVs than Physical Register mode can support, and are submitted for Conformance after 1-Aug-2002, must support Direct Mode. If the decoder supports Direct CV Addressing, the decoder also needs to support Address-Only programming. The manufacturer must clearly label, using the terms described in this Standard, which form(s) of programming are supported.

For complete backward compatibility with Command Stations or Programmers that were produced prior to 1-Aug-2002 which do not support direct mode, support for paged mode is strongly encouraged.

All programmable decoders must support Direct mode. Other modes are optional, but it is strongly recommended for backwards compatibility reasons, that the other modes are supported, particularly Page mode.

6 APPENDIX A: Address Query Instruction

The Address Query instruction is used in older Digital Decoders to verify a specific decoder address, CV #1. The format of the instruction is:

```
long-preamble 0 AAAAAAAA 0 11111001 0 EEEEEEEE 1
```

If the address in the packet matches the address of the Digital Decoder, the Digital Decoder generates an acknowledgment as specified in Section 3. This instruction is included to allow Programmers to verify addresses of older decoders. It is recommended that a Programmer first attempt to read CV# 1 with the Direct or Paged verify mechanism before invoking this method of Address Query. After unsuccessfully attempting to read the value of CV# 1, it can be verified to match the address of the Decoder using this Address Query command. This Address Query Instruction may only be issued for the Address range of AAAAAAAA from 1 to 111 decimal.

7 APPENDIX B: Service Mode Decoder Lock Instruction

This Appendix contains the definition of an additional instruction. A DCC product need not implement the feature described in this Appendix, but if it is implemented, it must be implemented completely.

Commented [MM9]: I want to remove these two paras, and replace with the para below. 2 Aug 2002 is now 24 years ago.

Commented [MJ10R9]: Agreed

Commented [MM11]: Do we still need to retain this requirement in Command Stations/Programmers? It may have been required in the last millennium, but is it still relevant now? It refers to "older" decoders, without explaining what they are. I don't know in 2026 what those "older" decoders might be, so I guess nobody else does either.

Commented [MJ12R11]: Another good question to put out for the DCC WG

Commented [MM13]: Is this another requirement that time has passed by? Can we remove it now? This is what CV15/16 is used for now, and arguably these do a better job than this which is an entirely transient service-mode-only thing in that its unlocked by any operations mode packet.

Commented [MJ14R13]: Absolutely

Additional information is available in Technical Note TN-2-05.

Commented [MM15]: No longer available.

Commented [MJ16R15]: Probably outdated. I have a draft copy from long ago. I will attach it, but likely of no use.

The Service Mode Decoder Lock instruction prevents service mode programming of some decoders, while allowing programming of others on a single track. Note: This is not a substitute for a low current programming track for new decoder instructions. Command stations/programmers must contain clear instructions on how to install and utilize a low current programming track.

The format of the instruction is:

```
long-preamble 0 00000000 0 11111001 0 0aaaaaaa 0 EEEEEEEE 1
```

Where “aaaaaaa” is the short address of the decoder that will continue to execute service mode commands.

Upon receiving a 0xF9 Service Mode Decoder Lock instruction, a decoder which implements this feature will check its address against the short address contained in the packet (“aaaaaaa”). If its address does not match the address in the packet, the decoder will be considered locked and will ignore all subsequent service mode instructions (even after a power cycle).

To unlock a decoder that has been locked using the Service Mode Decoder Lock instruction, the decoder must receive a valid NMRA DCC packet other than either a valid service mode packet or a valid Service Mode Decoder Lock instruction (with an “aaaaaaa” that does not match its address). Once unlocked, the decoder will accept all subsequent service mode packets.

8 Document History

Date	Description
1999	Initial release as RP-9.2.3
2006	Modified, details unknown.
2026	Reformatted, reviewed. Many small editorial changes. Changes to the status of the para referencing changes to CV1, and changes suggested to support for modes other than Direct mode. Questions asked about “older” decoders and suchlike. Recommendation to remove Appendixes A and B. M Moignard

Important Notices and Disclaimers Concerning NMRA Standards Documents

The Standards (S), Recommended Practices (RP), Technical Note (TN), and Technical Information (TI) documents of the National Model Railroad Association ("NMRA Standards documents") are made available for use subject to important notices and legal disclaimers. These notices and disclaimers, or a reference to this page, appear in all standards and may be found under the heading "Important Notices and Disclaimers Concerning NMRA Standards Documents."

Notice and Disclaimer of Liability Concerning the Use of NMRA Standards Documents

NMRA Standards documents are developed within the Standards and Conformance Department of the NMRA in association with certain Working Groups, members, and representatives of manufacturers and sellers. NMRA develops its standards through a consensus development process, which brings together volunteers representing varied viewpoints and interests to achieve the final product. NMRA Standards documents are developed by volunteers with modeling, railroading, engineering, and industry-based expertise. Volunteers are not necessarily members of NMRA, and participate without compensation from NMRA.

NMRA does not warrant or represent the accuracy or completeness of the material contained in NMRA Standards documents, and expressly disclaims all warranties (express, implied and statutory) not included in this or any other document relating to the standard or recommended practice, including, but not limited to, the warranties of: merchantability; fitness for a particular purpose; non-infringement; and quality, accuracy, effectiveness, currency, or completeness of material. In addition, NMRA disclaims any and all conditions relating to results and workmanlike effort. In addition, NMRA does not warrant or represent that the use of the material contained in NMRA Standards documents is free from patent infringement. NMRA Standards documents are supplied "AS IS" and "WITH ALL FAULTS."

Use of NMRA Standards documents is wholly voluntary. The existence of an NMRA Standard or Recommended Practice does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the NMRA Standards documents. Furthermore, the viewpoint expressed at the time that NMRA approves or issues a Standard or Recommended Practice is subject to change brought about through developments in the state of the art and comments received from users of NMRA Standards documents.

In publishing and making its standards available, NMRA is not suggesting or rendering professional or other services for, or on behalf of, any person or entity, nor is NMRA undertaking to perform any duty owed by any other person or entity to another. Any person utilizing any NMRA Standards document, should rely upon their own independent judgment in the exercise of reasonable care in any given circumstances or, as appropriate, seek the advice of a competent professional in determining the appropriateness of a given NMRA Standards document.

IN NO EVENT SHALL NMRA BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO: THE NEED TO PROCURE SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE PUBLICATION, USE OF, OR RELIANCE UPON ANY STANDARD OR RECOMMENDED PRACTICE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE AND REGARDLESS OF WHETHER SUCH DAMAGE WAS FORESEEABLE.

Translations

NMRA's development of NMRA Standards documents involves the review of documents in English only. In the event that an NMRA Standards document is translated, only the English version published by NMRA is the approved NMRA Standards document.

Official Statements

A statement, written or oral, that is not processed in accordance with NMRA policies for distribution of NMRA communications, or approved by the Board of Directors, an officer or committee chairperson, shall not be considered or inferred to be the official position of NMRA or any of its committees and shall not be considered to be, nor be relied upon as, a formal position of NMRA.

Comments on Standards

Comments for revision of NMRA Standards documents are welcome from any interested party, regardless of membership. However, **NMRA does not provide interpretations, consulting information, or advice pertaining to NMRA Standards documents.**

Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Since NMRA standards represent a consensus of concerned interests, it is important that any responses to comments and questions also receive the concurrence of a balance of interests. For this reason, NMRA, its departments, Working Groups or committees cannot provide an instant response to comments, or questions except in those cases where the matter has previously been addressed. For the same reason, NMRA does not respond to interpretation requests. Any person who would like to participate in evaluating comments or in revisions to NMRA Standards documents may request participation in the relevant NMRA working group.

Laws & Regulations

Users of NMRA Standards documents should consult all applicable laws and regulations. Compliance with the provisions of any NMRA Standards document does not constitute compliance to any applicable regulatory requirements. Implementers of the standard are responsible for observing or referring to the applicable regulatory requirements. NMRA does not, by the publication of NMRA Standards documents, intend to urge action that is not in compliance with applicable laws, and NMRA Standards documents may not be construed as doing so.

Copyrights

NMRA Standards documents are copyrighted by NMRA under US and international copyright laws. They are made available by NMRA and are adopted for a wide variety of both public and private uses. These include both use, by reference, in laws and regulations, and use in private self-regulation, standardization, and the promotion of modeling, structural and engineering practices and methods. By making NMRA Standards documents available for use and adoption by public authorities and private users, NMRA does not waive any rights in copyright to the NMRA Standards documents.

IMPORTANT NOTICE

NMRA Standards documents do not guarantee or ensure safety, security, health, or environmental protection, or ensure against interference with or from other systems, devices or networks. NMRA Standards documents development activities consider research and information presented to the standards development group in developing any safety recommendations. Other information about safety practices, changes in technology or technology implementation, or impact by peripheral systems also may be pertinent to safety considerations during implementation of the standard. Implementers and users of NMRA Standards documents are responsible for determining and complying with all appropriate safety, security, environmental, health, and interference protection practices and all applicable laws and regulations.